Additional Instruction to Part 4, Project-1

1. Before you begin:
   1. Do either
      1. Replace your mem.vhd with the revised one, or
      2. From the revised memory design, copy the two lines followed by “--newly added” and paste them in the mem.vhd that you have been using.
   2. Put the dmem.mif in the working directory. // it’s for memory initialization
   3. Modify your top-level design (i.e., the final product of Part 3, Project-1) such that it has an output port of std\_logic\_vector(31 downto 0). Let mem.q be the driver of the output. *If your top-level design already has one or more output ports, you can skip this step.* This additional output port is of no use, but it’s an effective trick to avoid optimization.
2. Follow the steps (a) and (b) in the lab manual.
   1. If Quartus doesn’t compile and return an error saying *“…Can’t find database file…”* copy the entire working directory and put it under the local C drive, C:\.
   2. Compilation does take some time (10+ minutes).
3. Additional notes for the rest of the semester
   1. Please avoid using process (or behavioral modeling style) as much as possible, except the testbench--some behavioral designs are not synthesizable.